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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,053	09/05/2003	SHIOU-JE LIN	9719-US-PA	2052

31561 7590 04/06/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
FARROKH, HASHEM	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,053	LIN ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 14-16* is/are rejected.

7)☒ Claim(s) *5-13,17-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the Applicant's Remarks dated January 27, 2006. The instant application having application No. 10/605,053 has a total of 21 claims pending in the application; no claims have been amended, added, canceled.

INFORMATION CONCERNING CLAIMS:

Claim Objections

Claim 1 is objected to because of the following informalities:

The period (.) in line 12 of claim 1 is improper.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

Claims 1-3, 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,052,767 to Matuki.

1. In regard to claim 1, Matuki teaches:

"A memory architecture used to repair a serial access memory comprising a main memory **(e.g., see title; column 1, lines 7-11; column 2, lines 25-27; element 39 In Fig. 6)**, a redundant memory and a control interface circuit **(elements 23, 41, and 43 in**

Fig. 6), the control interface circuit storing a plurality of addresses **(element 15 in Fig. 2; element 25 in Fig. 7)**, each of the addresses corresponding to a damaged memory cell in the main memory **(column 4, lines 6-33)**, when the memory module is accessed by an access address **(SERIAL ADDRESS in Fig. 6)**, the control interface circuit issuing a pointer address pointing to a corresponding address in the stored addresses in the control interface circuit and comparing the address corresponding to the pointer address and the access address;" **(e.g., see title; column 5, lines 64-67 to column 6, lines 1-15; Figs. 6-7).** *Matuki teaches a system and method for repairing or replacing defective memory in a serially access memory. The address or locations of predetermined defective memory cells are stored in a fuse box. The internally generated address of defective memory cells is first converted from parallel to serial and the compared by a comparator (e.g., element 29 in Figs. 6-7) to the serial input address.*

"if the address corresponding to the pointer address is equal to the access address **(column 6 lines 54-58)**, data accessed by the access address from the memory module is read out from the redundant memory." **(e.g., see column 8 lines 15-19).**

2. *In regard to claim 2, Matuki teaches:*

"the data accessed by the access address from the memory module being read out from a memory address of the redundant memory **(claim 1)**, the memory address corresponding to the pointer address issued by the control interface circuit." **(e.g., see column 5 lines 28-47; Fig. 6).** *For example the address stored in buffer 31 shown in*

Fig. 6 is used to access memory cell array 39 (e.g. main memory) or redundant memory depending on the state of memory select signal.

3. In regard to claim 3, Matuki teaches:

"each of the addresses stored in the control interface circuit having a memory address that corresponds to the redundant memory **(column 4, lines 6-32)**, if the address corresponding to the pointer address is equal to the access address **(column 4, lines 47-57))**, the data read out from the memory address of the redundant memory corresponds to the address." **(e.g., see claim 1).**

4. In regard to claim 14, Matuki teaches:

"A method for repairing a serial access memory **(e.g., see title; column 1, lines 7-11; column 2, lines 25-27)**, the memory module comprising a main memory **(element 39 in Fig. 6)**, a redundant memory and a control interface circuit **(elements 23, 41, and 43 in Fig. 6)**, the control interface circuit for storing a plurality of addresses **(element 15 in Fig. 2; element 25 in Fig. 7)**, each of the addresses corresponding to a damaged memory cell in the main memory **(column 4, lines 6-33)**, assessing the memory module by an access address;" **(e.g., see claim 1).**

"issuing a pointer address by the control interface circuit to point to a corresponding one of the stored addresses stored in the control interface circuit;" **(e.g., see column 5 lines 64-67 to column 6, lines 1-11; Fig. 7).** *The memory selective unit 23 represents the control interface circuit recited in the claim which retrieves the internally stored defective*

address (e.g. X1-X4). The stored defective address are inherently are pointed (e.g., addressed) by the memory selective unit 23.

"comparing the address corresponding to the pointer address and the access address **(column 6, lines8-10; element 29 in Fig. 7)**, if the address corresponding to the pointer address is equal to the access address **(column 6 lines 54-58)**, data accessed by the access address from the memory module being read out from the redundant memory." **(e.g., see column 8 lines 15-19).**

5. *In regard to claim 15, Matuki teaches:*

"wherein the memory address corresponds to the pointer address issued by the control interface circuit." **(e.g., see column 5 lines 64-67 to column 6, lines 1-11; Fig. 7).** *The memory selective unit 23 represents the control interface circuit recited in the claim which retrieves the internally stored defective addresses (e.g. X1-X4). The stored defective address are inherently are pointed (e.g., addressed) by the memory selective unit 23.*

6. *In regard to claim 16, Matuki teaches:*

"wherein if the redundant selection signal is activated **(e.g., see column 6, lines 53-58)**, the data accessed by the access address from the memory module is read out from the redundant memory **(e.g., see claim 1)**, if the redundant selection signal being not activated **(e.g., see column 7, lines 1-6)**, the data accessed by the access address from the memory module is read out from the main memory." **(e.g., see claim 1).** *For example when the memory Select is high (e.g., activated) the data is access from*

redundant memory. If the memory Select is low (e.g., inactive) the data is access from main memory.

ALLOWABLE SUBJECT MATTER

Claims 4-13, and 17-21 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claims 4-12 in instant application is the combination with the inclusion of the following limitation: **A fuse box, coupled to the pointer control unit registering the addresses of the damaged cells of the main memory and outputting one of the addresses according to the pointer address.**

2. The primary reason for allowance of claims 17-18 in instant application is the combination with the inclusion of the following limitation: **wherein the pointer control unit increments the pointer address by a step value when the redundant selection signal is set.**

3. The primary reason for allowance of claims 19-20 in instant application is the combination with the inclusion of the following limitation: **wherein the pointer control unit decrements the pointer address by a step value when the redundant selection signal is set.**

4. The primary reason for allowance of claims 13 and 21 in instant application is the combination with the inclusion of the following limitation: **wherein the main memory is a first-in-first-out memory circuit.**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Response to Applicant's Remarks

The Applicant's Remarks has been carefully reviewed by the Examiner and is persuasive. Therefore, a different prior art reference is used to overcome the Applicant's arguments.

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 6,768,694 B2 to Anand et al. Method of electrically blowing fuses under control of an on-chip tester interface apparatus.

2. U. S. Patent No. 6,336,176 B1 to Leydaet al. describes Memory configuration data protection.

3. U. S. Patent No. 5,604,702 A to Tailliet describes Dynamic redundancy circuit for memory in integrated circuit form.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

~~HF~~
HF

2006-04-01

DONALD SPARKS
SUPERVISORY PATENT EXAMINER